

PY32F420RxT-START V2

User Guide



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Contents

1.	Introduction	3
2.	Functional pin assignment.....	4
3.	Overview of Hardware Design	5
3.1	Power Supply.....	5
3.2	I _{DD} TEST	6
3.3	LED Indicator Light	6
3.4	Reset Key.....	7
3.5	User Key.....	7
3.6	Boot Mode Selection	8
3.7	External Clock Source.....	8
3.8	Programming and debugging:.....	9
3.9	Vrefbuf	10
4.	Guide to Using the Example	11
4.1	LED Example.....	11
4.2	KEY Example.....	11
4.3	FLASH Example.....	11
5.	Schematic	12
5.1	PY-LINK Schematic.....	12
5.2	MCU Schematic	13
6.	Updated History	14

Figure 1-1 PCB 3D renderings

2. Functional pin assignment

Table 2-1 Pin Assignment

Function	Pin	Description	Note
LED	\	LED1	PY-LINK LED
	\	LED2	VDD*
	PB2	LED3	User LED
KEY	\	K1	PY-LINK Key
	PB0	K2	User Key
	PD11	K3	Reset Key
SPI	PB12	SPI_NSS	ExternalFLASH
	PB13	SPI_CLK	ExternalFLASH
	PB14	SPI_MISO	ExternalFLASH
	PB15	SPI_MOSI	ExternalFLASH

3. Overview of Hardware Design

The development board is powered via a Type-C USB connection. To download programs to the board, a Type-C USB cable is required. Select the correct boot mode, connect the USB cable, and if LED1 lights up, it indicates a proper power connection.

3.1 Power Supply

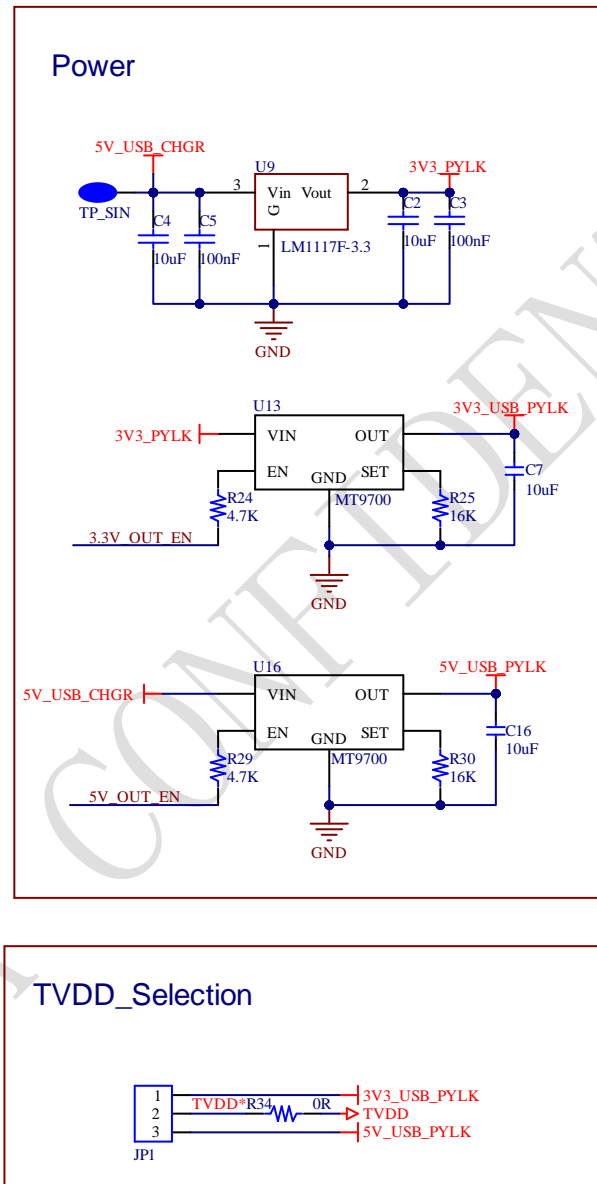


Figure 3-1 Power Supply Schematic

3.2 I_{DD} TEST

When JP2 OFF (symbol IDD) and R37 OFF, an ammeter can be connected to measure the power consumption of MCU.

JP2 OFF, R37 ON:MCU is powered. (Default setting and JP2 plug is not mounted before shipping)

JP2 ON, R37 OFF:MCU is powered.

JP2 OFF, R37 OFF:An ammeter must be connected. If there is no ammeter available, the MCU cannot be powered.

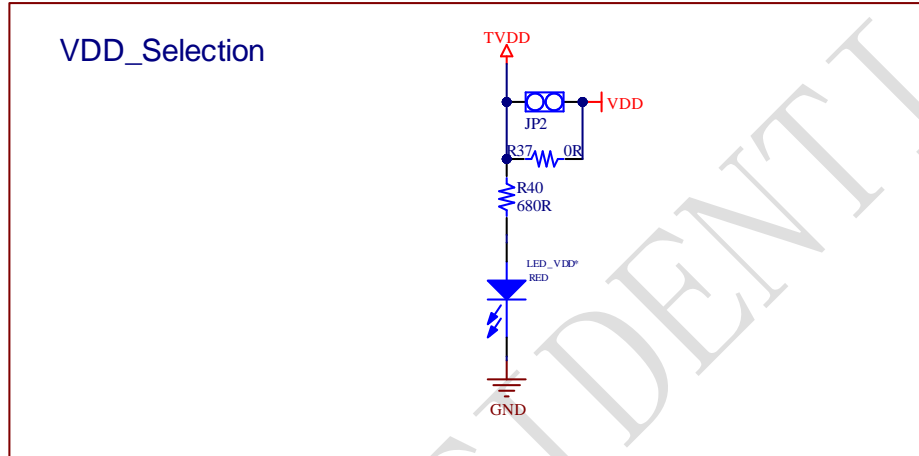


Figure 3-2 I_{DD} Schematic

3.3 LED Indicator Light

The red LED indicates that the board TVDD is powered as shown in the figure above; The green LED is the user LED connected to the PB2 pin of the MCU.

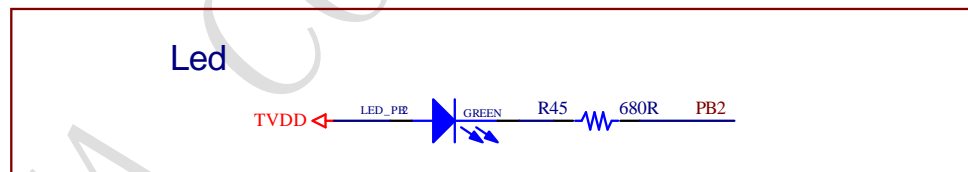


Figure 3-3 LED Schematic

3.4 Reset Key

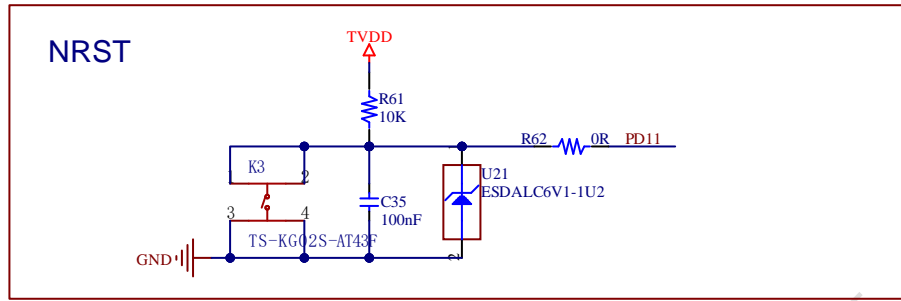


Figure 3-4 Reset Key Schematic

3.5 User Key

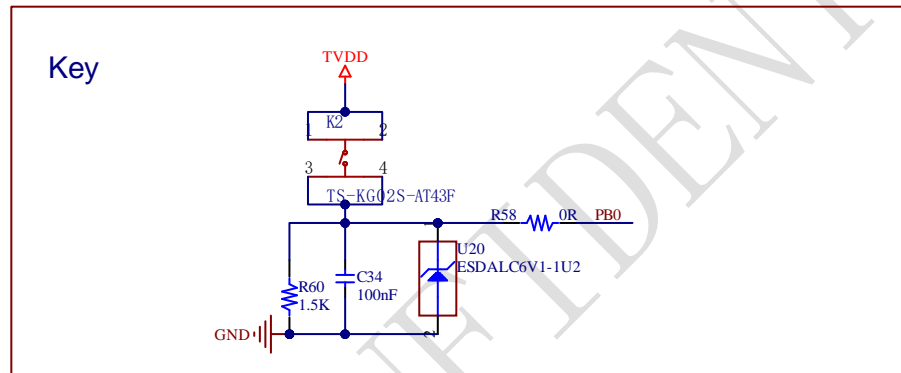


Figure 3-5 User Key Schematic

3.6 Boot Mode Selection

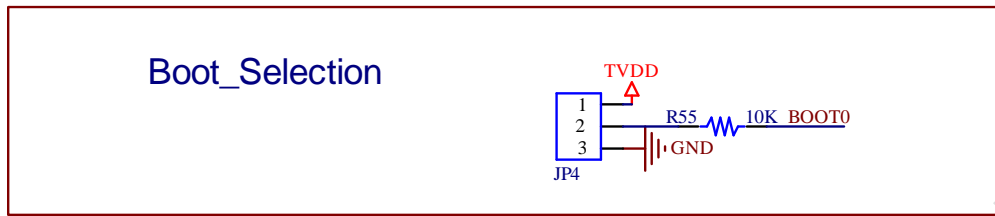


Figure 3-6 BOOT Mode Schematic

The boot mode can be selected among three different options by configuring the BOOT0 pin and Option Bytes, as shown in the following table:

Table 3-1 Boot configuration

Boot mode configuration					Mode
BOOT_LOCK	nBOOT1 FLASH_OPTR1[17]	nBOOT0 FLASH_OPTR1[16]	BOOT0 Pin	nSWBOOT0 FLASH_OPTR1[18]	
1	X	X	X	X	Select Main flash as the boot area
0	X	X	0	1	Select Main flash as the boot area
0	X	1	X	0	Select Main flash as the boot area
0	0	X	1	1	Select SRAM memory as the boot area
0	0	0	X	0	Select SRAM memory as the boot area
0	1	X	1	1	Select System memory as the boot area
0	1	0	X	0	Select System memory as the boot area

3.7 External Clock Source

HSE clock source

There are three methods to configure the external low-speed clock sources by hardware:

On-board crystal (Factory default setting):

On-board 24 MHz crystal is used as HSE clock source.

Oscillator from external PD0:

External oscillator is injected from the PD0 of CN3. The hardware must be configured: R53 OFF.

HSE unused

MCU PD0 and PD1 are used as GPIOs.

LSE clock source

There are three methods to configure the external low-speed clock sources by hardware:

On-board crystal (Factory default setting):

On-board 32.768 kHz crystal is used as HSE clock source.

Oscillator from external PC14:

External oscillator is injected from the PC14 of CN3. The hardware must be configured: R57 OFF.

LSE unused

MCU PC14 and PC15 are used as GPIOs.

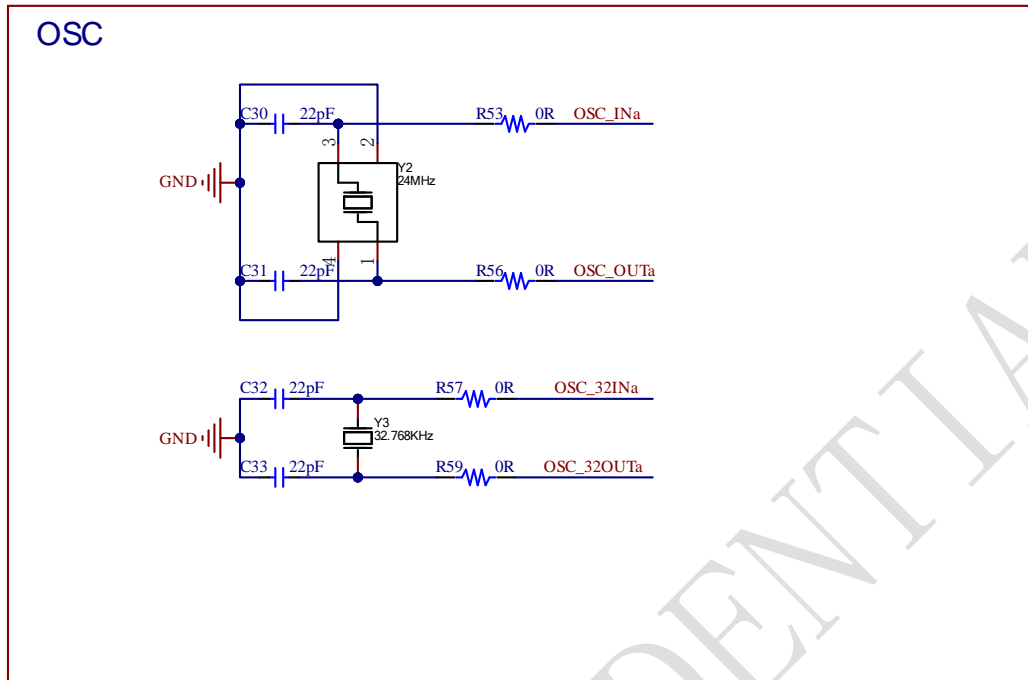


Figure 3-7 Clock source function schematic

3.8 Programming and debugging:

The evaluation board integrates PY-LINK for users to program/debug the PY32F420RxT on the PY32F420RxT-START V2 board. PY-LINK supports SWD interface mode, and supports a set of virtual serial ports (VCP) and PY32F420RxT's USART1_TX/USART1_RX (PA9/PA10) to connect and communicate through Dupont wire, please refer <USART> to the official PY32xxxx_Firmware Example. For more information about PY-LINK operation, firmware upgrade, and precautions, please refer to the "PY-LINK OB_UserManual_EN.pdf" document. The PY-LINK on board can be disassembled or separated from the PY32F420RxT-START V2. In this case, the PY32F420RxT-START V2 can still be connected to the CN1 interface of PY-LINK through CN5 interface (not mounted before leaving factory), or to another PY-LINK, in order to continue to program and debug the PY32F420RxT.

3.9 Vrefbuf

Use R63 OFF to achieve the Vrefbuf function of PA0 PIN.

R63 OFF: The PA0 PIN is used for the PA0 function. (This is the factory default setting. The R63 has not been installed.)

R63 ON: The PA0 PIN is externally connected with a 1uF capacitor to serve as the Vrefbuf function.

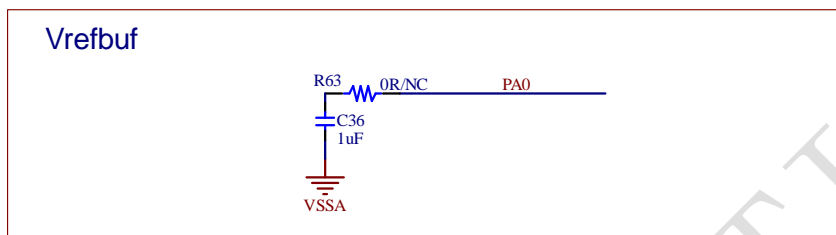


Figure 3-8 Vrefbuf schematic

4. Guide to Using the Example

4.1 LED Example

Purpose of the Example

There is one LED on the development board, the LED is controlled by GPIO. This sample program will tell how to light up the LED.

Execution Results

Download the official PY32xxxx_Firmware Example <GPIO_Toggle> to the board, reset and run, and the green LED flashes.

4.2 KEY Example

Purpose of the Example

There is 1 user button on the board. The user key is detected by the GPIO. This routine will show you how to detect a key with an external interrupt.

Execution Results

Download the official PY32xxxx_Firmware Example <EXTI_IT> to the board, reset and run, press the button once, and the green LED will switch to the on-off state once.

4.3 FLASH Example

Purpose of the Example

There is a flash on the development board, and the FLASH communication interface is connected to the SPI interface. This example will show you how to read and write FLASH via SPI.

Note:

1. The maximum working voltage of FLASH is 3.6V. It is recommended that the supply voltage of TVDD should not exceed 3.3V.

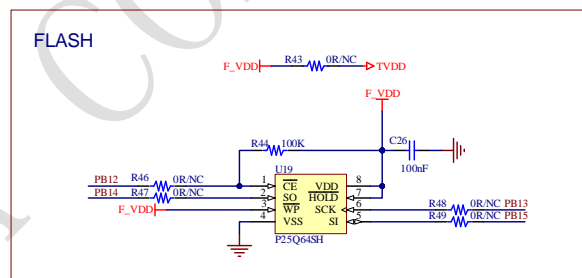


Figure 4-1 SPI-FLASH schematic

Execution Results

Download the official PY32xxxx_Firmware Example < SPI_FullDuplex_ExternalFLASH > to the board, reset and run, If the green LED is always on, the FLASH read and write is successful, otherwise the FLASH read and write fails.

5. Schematic

5.1 PY-LINK Schematic

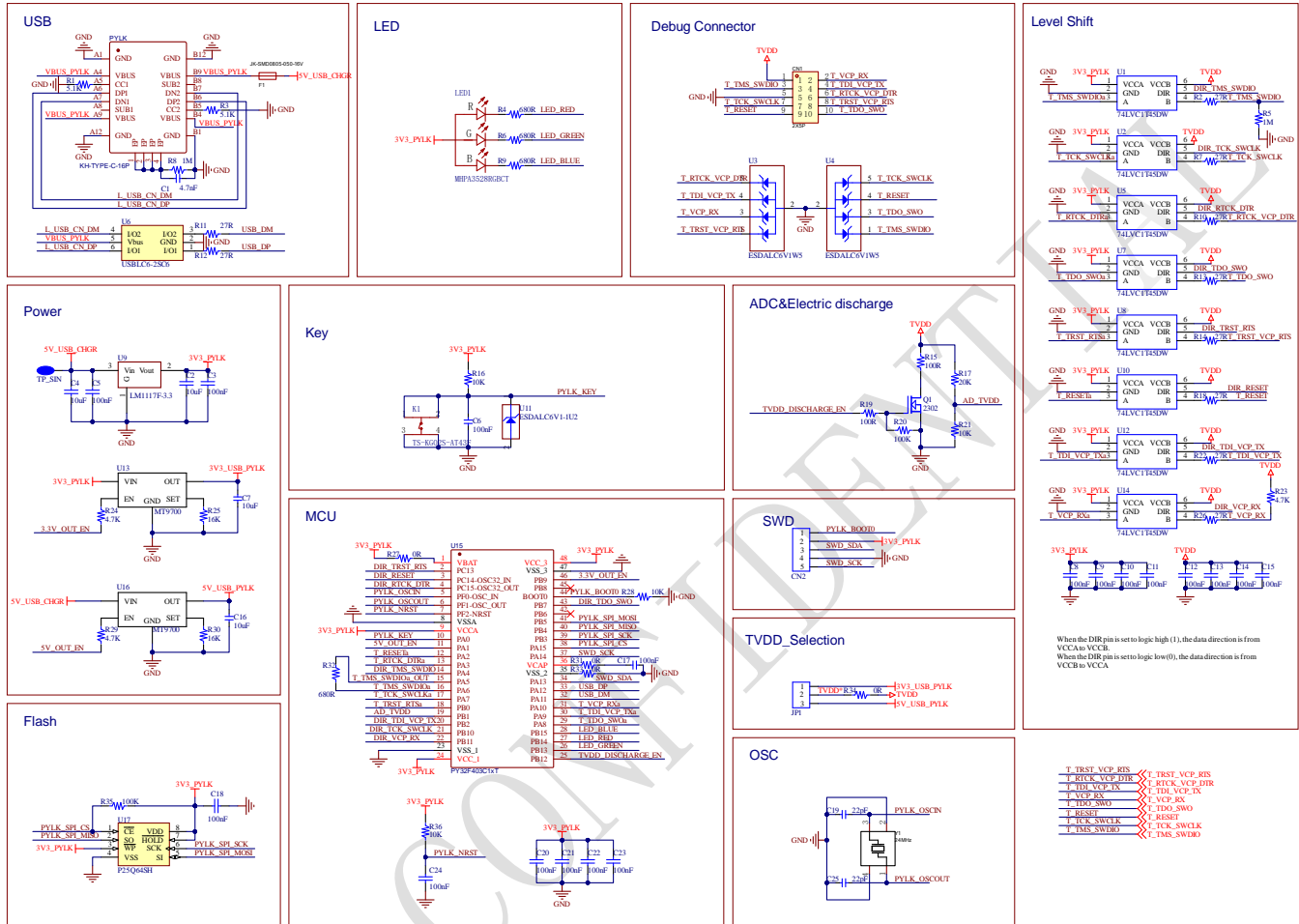


Figure 5-1 PY-LINK Schematic

5.2 MCU Schematic

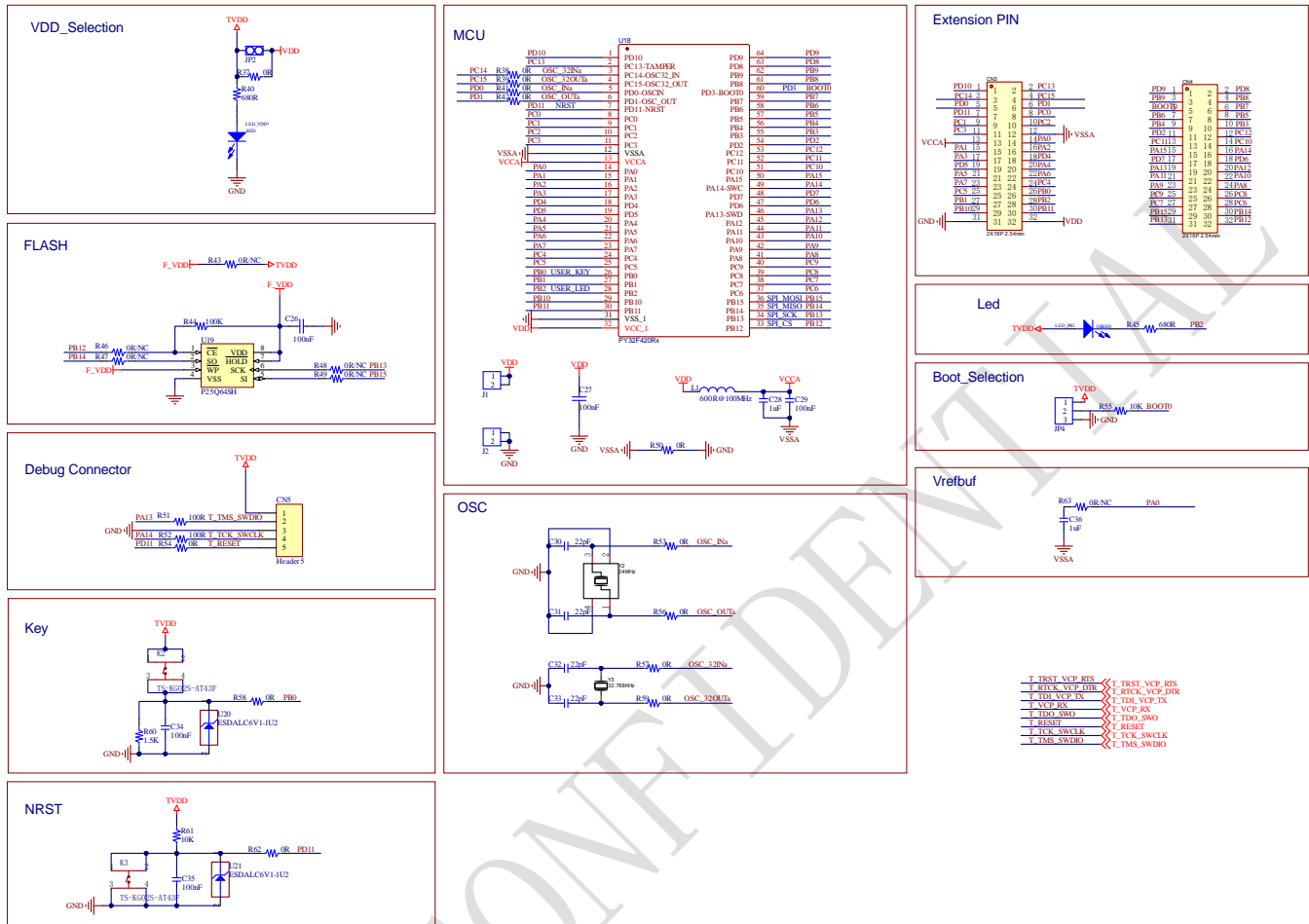


Figure 5-2 MCU Schematic

6. Updated History

Version	Content	Date
V1.0	Initial version	2026/04/01



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